	Туре	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	14	rost near timothy.in.	IH	2005/01/1 8 12:34
2	BRS	L2	52	burke near edmund.in.	US- PGPUB; USPAT;	2005/01/1 8 12:35
3	BRS	L3	374	438/250.ccls.	IH: D( ) •	2005/01/1 8 12 <b>:</b> 35

•	Туре	L #	Hits	Search Text	DBs	Time Stamp
4	BRS	L4	348	3 and capacitor	IH D( ) •	2005/01/1 8 12:49
5	BRS	L5	644	(capacitor) near25 (etch near stop)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 12:50
6	BRS	L6	44	(capacitor) near25 (etch near stop) near15 (protect\$3)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 13:02

	Туре	L #	Hits	Search Text	DBs	Time Stamp
7	BRS	L7	92	(interconnect\$1)	IH: D( ) •	2005/01/1 8 13:03
8	BRS	L8	247	(capacitor) near25 (etch\$3) near15 (interconnect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:47
9	BRS	L9	0	(capacitor) near25 ((protective near layer) near5 (etch\$3)) near15 (interconnect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14 <b>:</b> 28

	Туре	L #	Hits	Search Text	DBs	Time Stamp
10	BRS	L10		near15 (inter- connect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:28
11	BRS	L11	0	(capacitor) near25 ((protect near layer) near5 (etch\$3)) near15 (inter-connect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:28
12	BRS	L12	0	(capacitor) near25 ((protect near layer) near5 (etch\$3)) near15 (interconnect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:39

	Туре	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L13	1	<pre>(capacitor) near25 ((protect) near5 (etch\$3)) near15 (interconnect\$1)</pre>		2005/01/1 8 14:29
14	BRS	L14	0	<pre>(capacitor) near25 ((protect) near5 (etch\$3)) near15 (inter-connect\$1)</pre>	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:29
15	BRS	L15	115	<pre>(capacitor) near25 ((protect) near5 (etch\$3))</pre>	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:31

	Туре	L #	Hits	Search Text	DBs	Time Stamp
16	BRS	L16	13	(capacitor) near25 ((protect near layer) near5 (etch\$3))	IH: D( ) •	2005/01/1 8 14:29
17	BRS	L17	10	(capacitor) near25 ((protect) near5 (etch\$3)) near15 (metal)	IH: D( ) •	2005/01/1 8 14:33
18	BRS	L18	1247	<pre>(capacitor) near25 (etch\$3) same (protect\$3)</pre>	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:34

	Туре	L #	Hits	Search Text	DBs	Time Stamp
19	BRS	L19	19	((capacitor) near25 (etch\$3) near15 (interconnect\$1)) same (protect\$3)	1H' D( ) •	2005/01/1 8 14:34
20	BRS	L20	1075	((protect near layer) near5 (etch\$3))	IH. P( ) •	2005/01/1 8 14:40
21	BRS	L21	48	((protect near layer) near5 (etch\$3)) same (capacitor)	US- PGPUB; USPAT;	2005/01/1 8 14:40

	Туре	L #	Hits	Search Text	DBs	Time Stamp
22	BRS	L22	0	(capacitor) near25 (etch\$3) near15 (inter-connect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:47
23	BRS	L23	247	(capacitor) near25 (etch\$3) near15 (interconnect\$1)	US- PGPUB; USPAT; EPO; JPO; DERWE NT; IBM_T DB	2005/01/1 8 14:47

	υ	1	Document ID	Title	Current OR
1		l	US 20040087098 A1	MIM AND METAL RESISTOR FORMATION AT CU BEOL USING ONLY ONE EXTRA MASK	438/381
2		l	US 6730573 B1	MIM and metal resistor formation at CU beol using only one extra mask	438/381
3			US 6486530 B1	Integration of anodized metal capacitors and high temperature deposition capacitors	257/532
4			US 6284590 B1	Method to eliminate top metal corner shaping during bottom metal patterning for MIM capacitors	438/240
5			US 6239010 B1	Method for manually manufacturing capacitor	438/592

	U	1	Do	cument	ID	Title	Current	OR
6			US	446617	7 A	Storage capacitor optimization for one device FET dynamic RAM cell	438/251	
7			US	6430028	3 В	Metal-insulator-metal capacitor for use in semiconductor chips comprises spacer that protects dielectric layer from being etched		
8	X		US	6284590	) В	Fabrication of metal- insulator-metal capacitor used in radio frequency mixed signal applications involves anisotropically etching away flowable material layer as sidewall spacer of top metal electrode		
9	Х		US	6200905	5 В	Formation of sidewall capacitors while forming metal oxide semiconductor transistor gates involves etching away conductive sidewall spacers while protecting top plate with protective mask		
10	Χ		US	592401	l A	Fabrication of low resistance silicide for an analog/digital device		